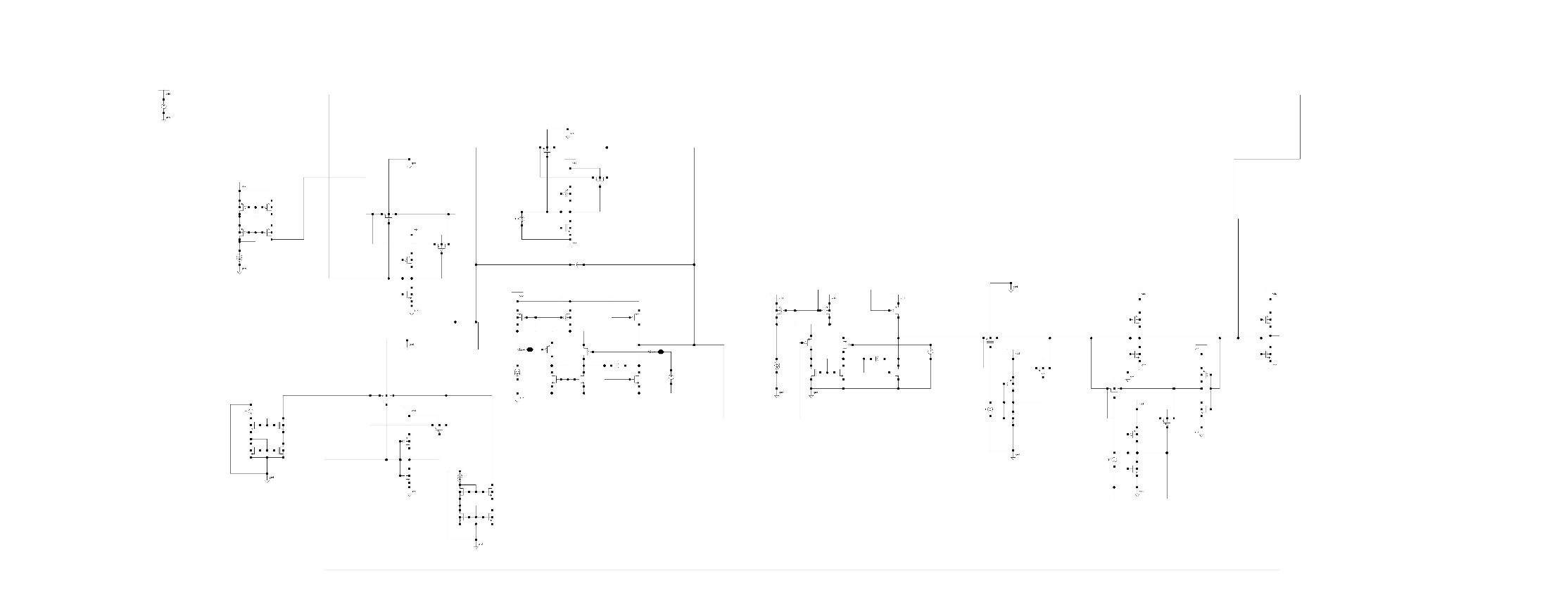
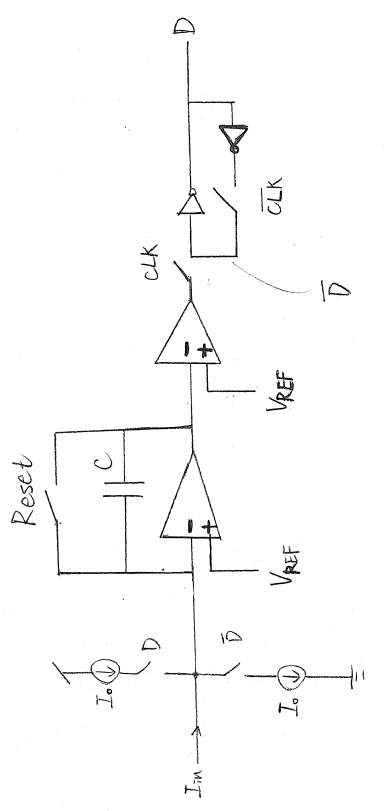
ESE 562\_Project 3

Po Hsu Chen, 448031

System level architecture with component values (C, Io, CLK, VREF, VCMP)

Vdd =3V



C feedback

C =3p

Amplifier 2

C =3 p

Idc=100m A

Vdc=1.5 V

Amplifier 1

C =11.5 p

Idc=100m A

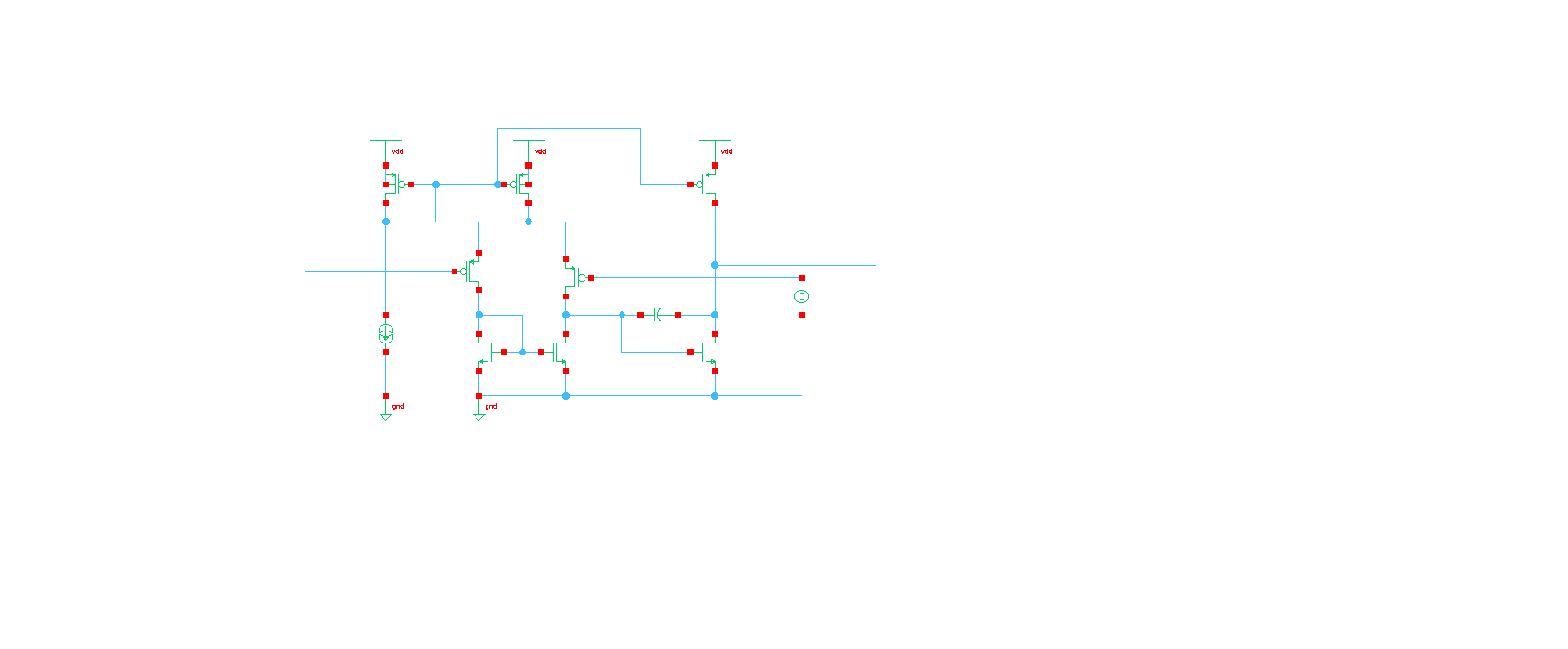
Vdc=1.5 V

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **C** | **Io** | **CLK** |  |  |
| 3p | 130n A | V pulse 0 ~ 3V (3~0V) | 1.5 V | 1.5 V |
|  |  | Pulse width 20u s |  |  |
|  |  | Period 40u s |  |  |

Amplifier Implementation

I chose the amplifier as the one in project 1.

Amplifier 1.

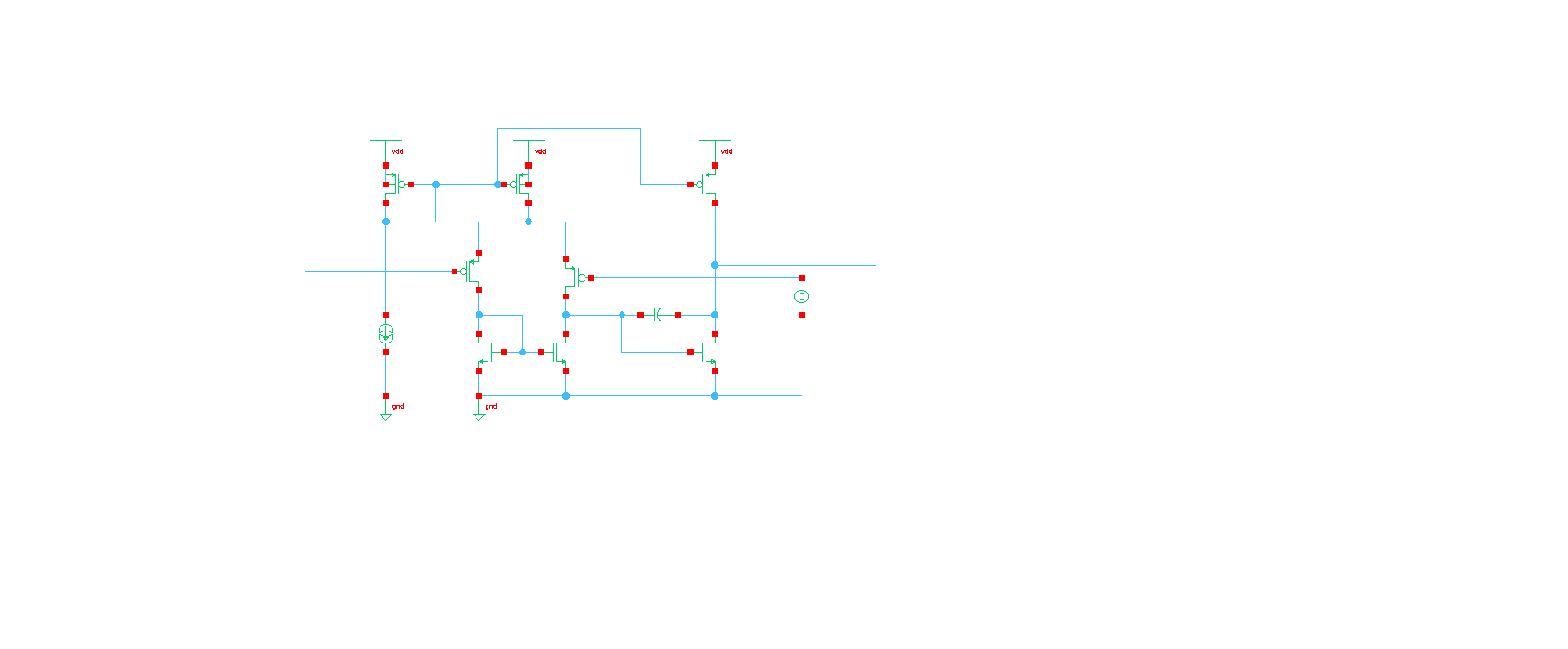


Idc = 100u A

Vdc = 1.5V

C=11.5 p

Amplifier 2.

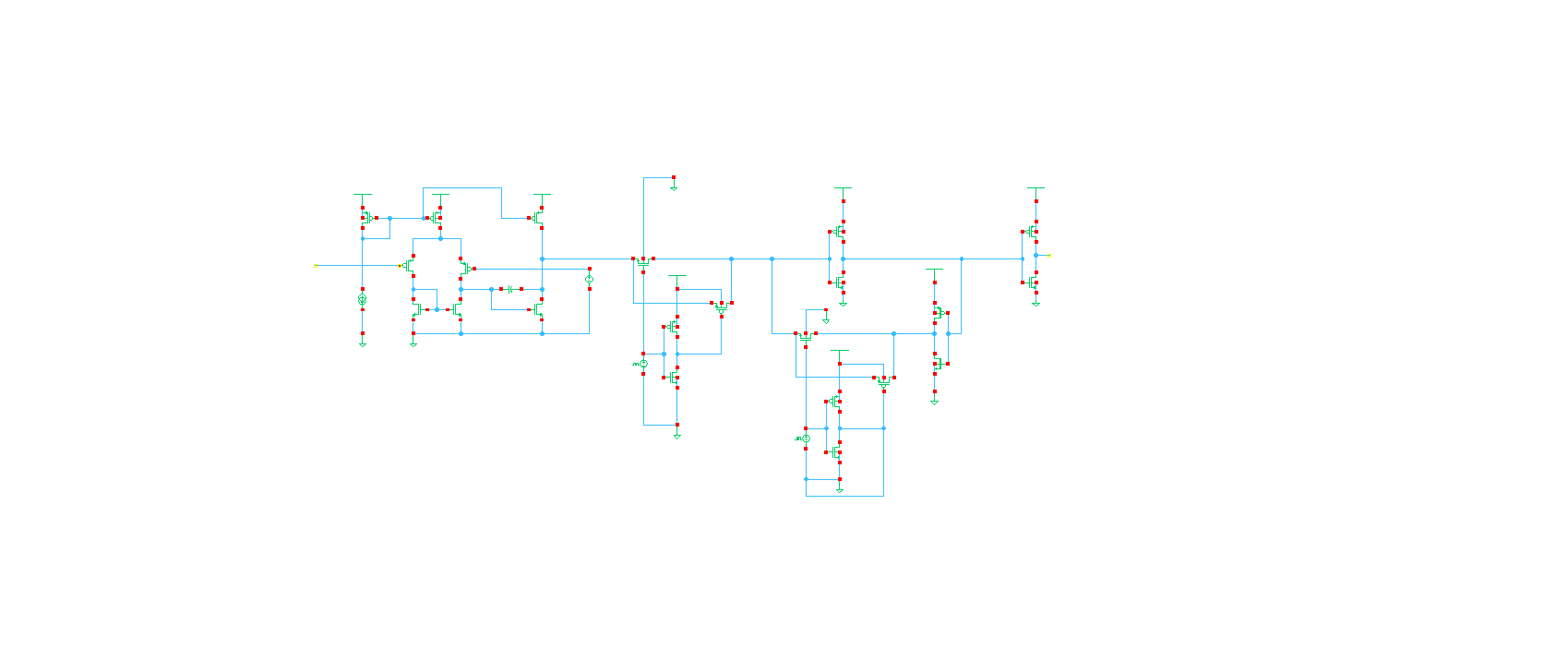


Vdc = 1.5V

C= 3p

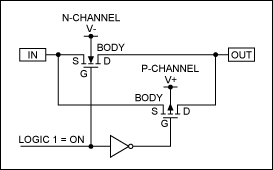
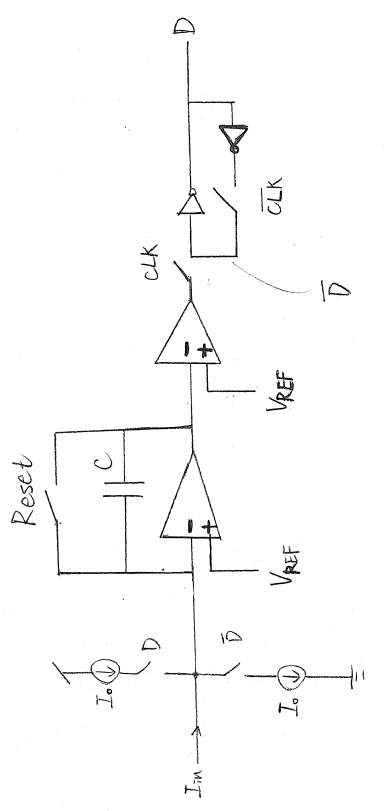
Idc = 100u A

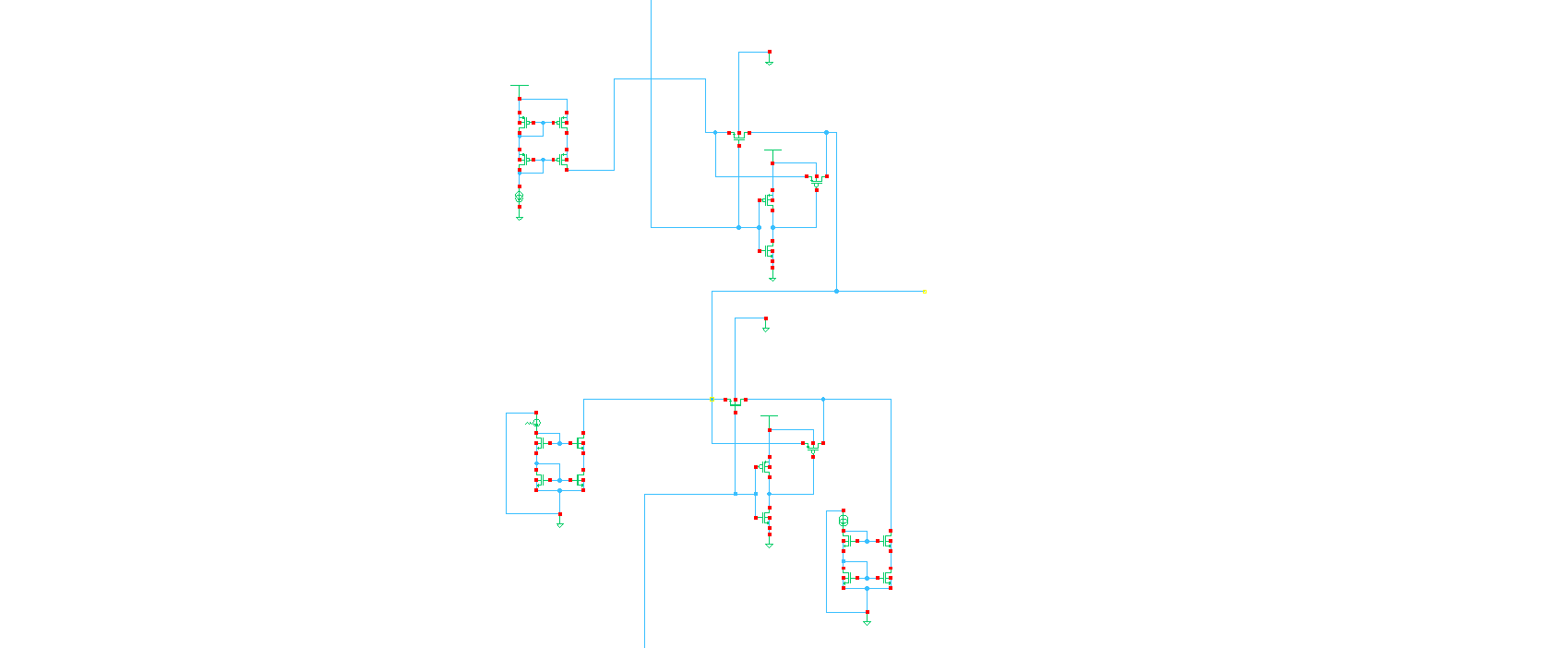
Implementation

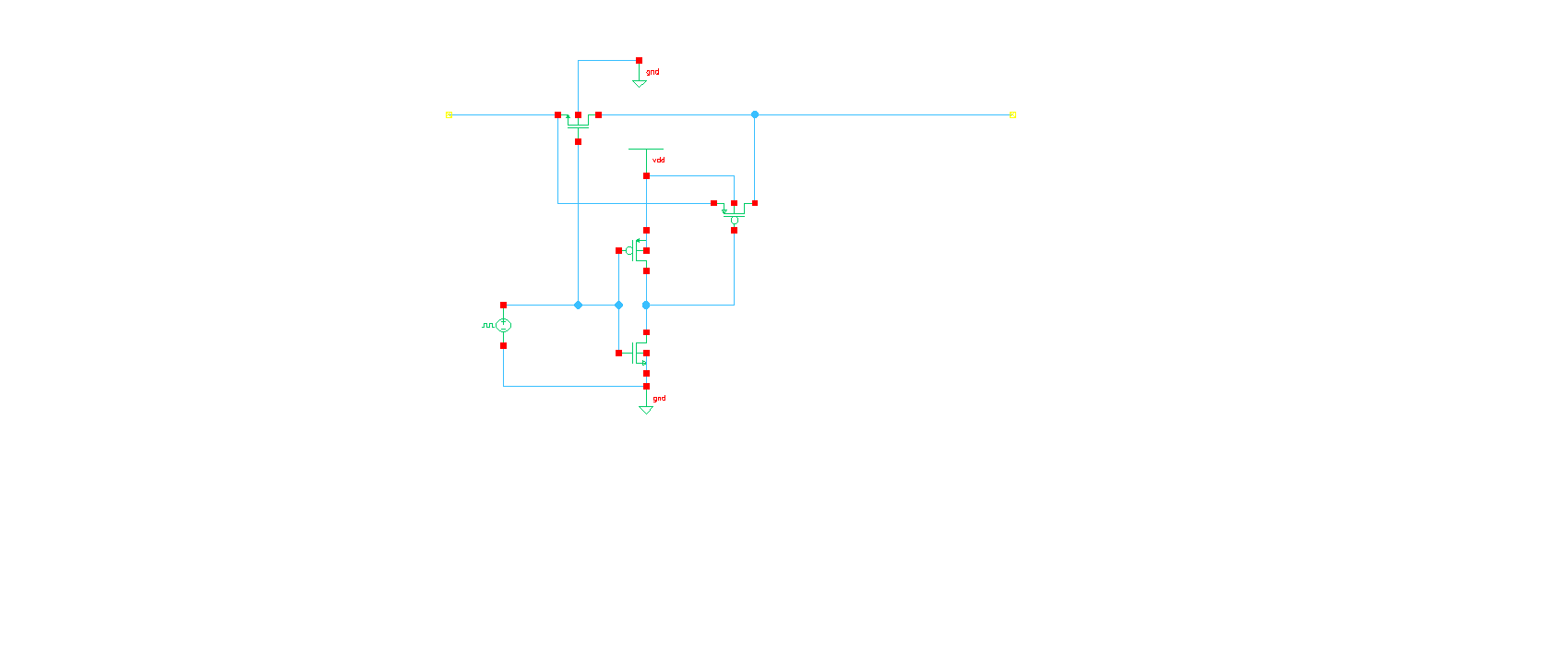


**CMOS Switch**

**Current Source and Sink**

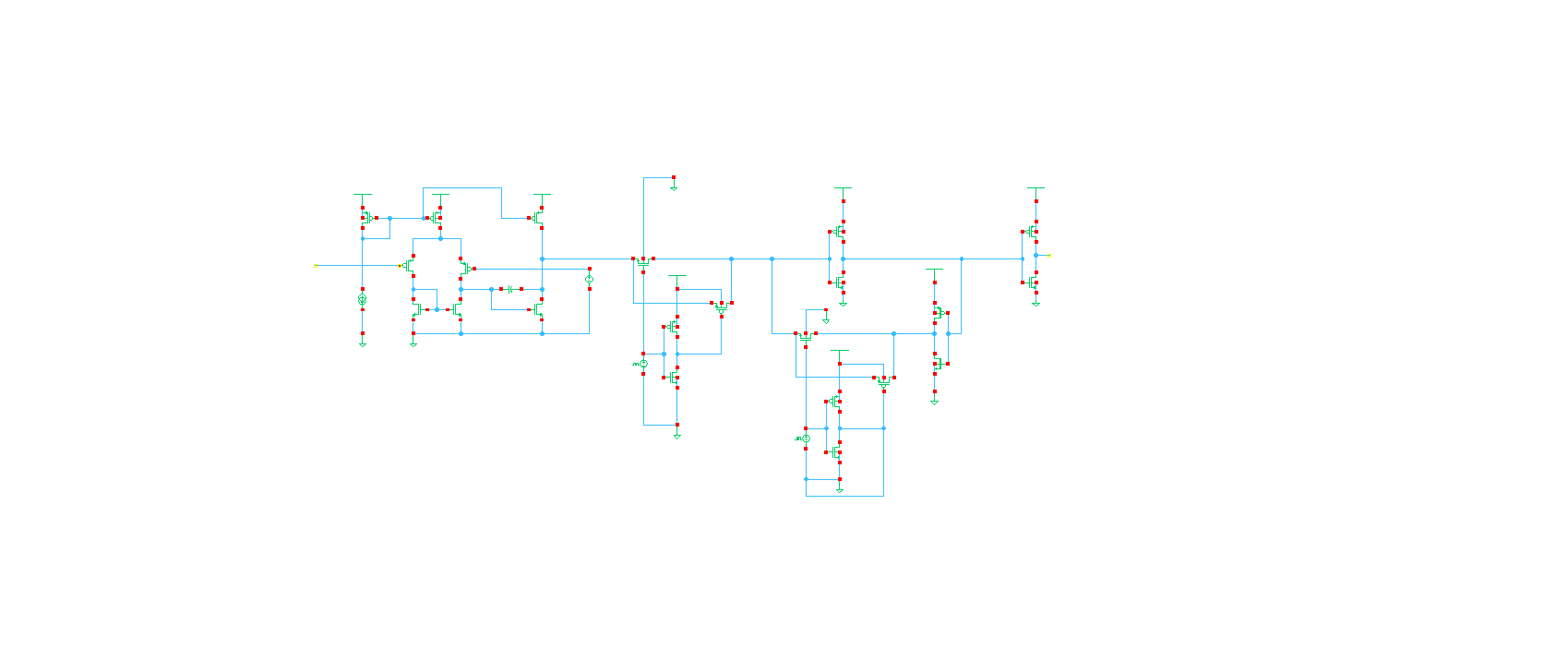






**Latched Comparator**





C=3p F

Idc=100u A

Vdc=1.5V

CLK is 3~0V

Pulse width 20u s

Period 40u s

CLK is 0~3V

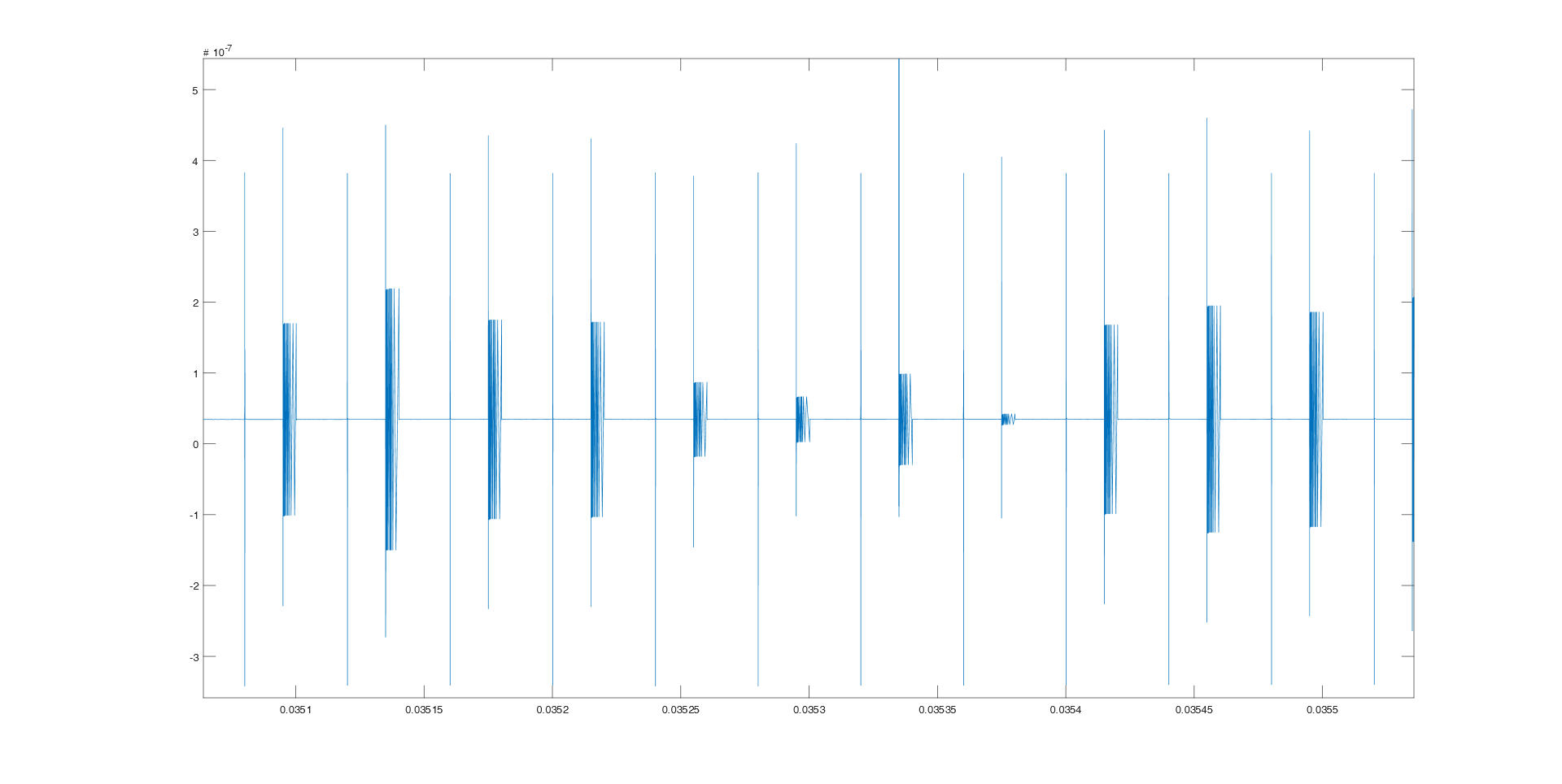
Pulse width 20u s

Period 40u s

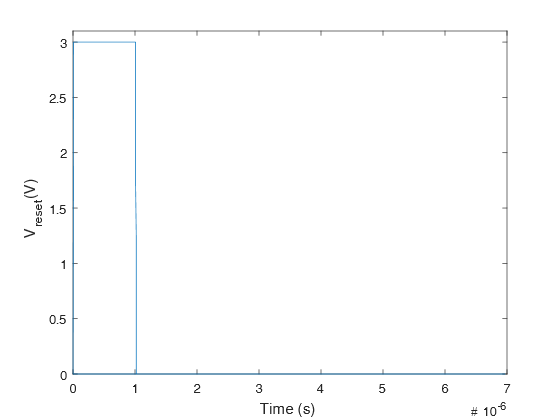
Output of the modulator and voltage Vx

Horizontal line = I\_in

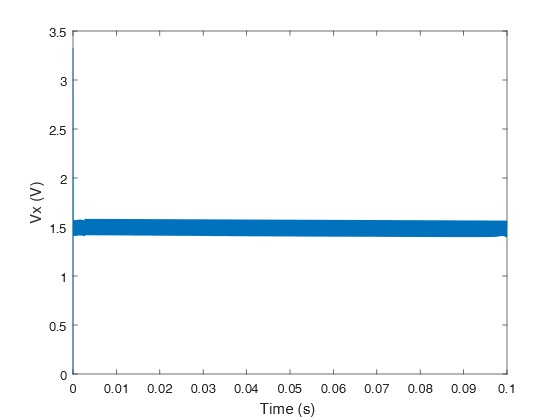
Switch spike

**Iin**

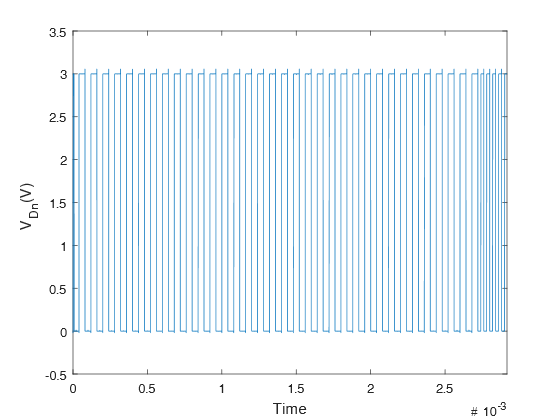
**V\_reset:**

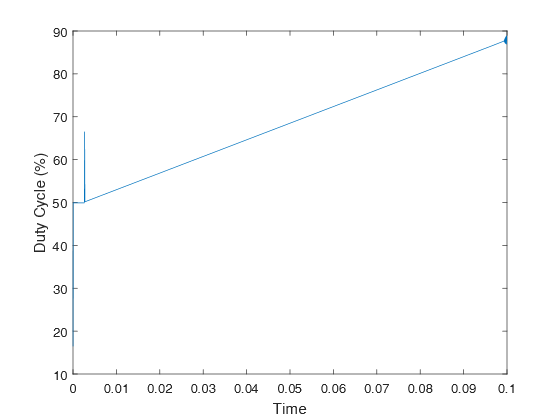


**Vx**



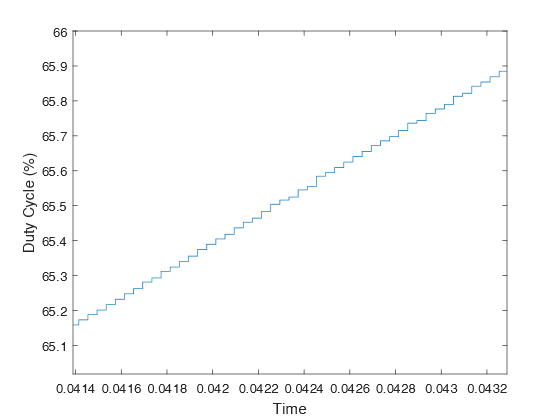
**V\_Dn and Duty Cycle**





**The wave form of output of initial state and the next state overlaps caused the duty cycle isn’t continuously.**

**Thus, there’s a spike here.**



**Reset spike**

**Speed:**

CLK is 0~3V and 3~0V

Pulse width 20u s

Period 40u s

**Resolution:**

Since there are 2410 data points in duty cycle.

=>The resolution is 11.2 bit.

**Power Dissipation:**

P = I\*V

P = 399u A\* 3 V = 1.2m Watt